CND 211
Advanced Digital Design
2023

Course Description

The main objective of this course is to introduce the students to advanced digital integrated circuit design with emphasis on “hands-on” digital IC design using modern CAD tools. The student will be introduced to the digital design flow for ASIC design including Verilog modelling, synthesis, timing analysis and constraints, clock synthesis, placement and routing, signal and power integrity issues, and design for testing.

Contact Hours

Credit Hours	Lecture Hours	Lab Hours	Student work	Total
6	24 (1.25x2)/week	33 (3x1)/week	48	93

Prerequisites

Introduction to Digital Design

Learning Outcomes

After successful completion of this course, the student will be able to:

1. Learn the full cycle of design of digital IC starting from defining specifications, functional design, design, synthesis, placement and routing, and layout to build a cell library.
2. Know how to use modern industrial EDA design tools to perform advanced circuit design.

References

- André Inácio Reis, Rolf Drechsler, Advanced Logic Synthesis, Springer International Publishing, 2018.
- Vaibbhav Taraate. Logic Synthesis and SOC Prototyping RTL Design using HDL. Springer
- A. Reis, R. Drechsler. Advanced Logic Synthesis. Springer; 2017
- Givanni De Micheli, “Synthesis & Optimization of Digital Circuits”. McGraw Hill, 2003.
- J. Bhasker, R. Chadha. Static Timing Analysis for Nanometer Designs: A Practical Approach. Springer; 2013
- Seongbo Shim, Youngsoo Shin. Physical Design and Mask Synthesis for Directed Self-Assembly Lithography. Springer. 2018
- Thomas Dillinger. VLSI Design Methodology Development. Prentice Hall, 2019.

- Joseph S. Valacich, Joey F. George , Jeff Hoffer. Essentials of Systems Analysis and Design. Pearson, 2015
- Material is also derived from the IEEE Journals, Transactions, and flagship Conference proceedings.

CAD Tools: Synopsys flow including

- Design Compiler for Synthesis.
- Formality for Formal Verification.
- Library Manager for Data Setup.
- ICC2 [IC Compiler 2] for floorplanning , power planning , placement, CTS, Routing.
- PrimeTime for STA

Course Project: By the end of this course the students are required to deliver a complete project (chosen from variety of proposals) assigned by the industry experts and university professors instructors.

Course Topics and Schedule

Week	Lecture	Lab
1	Introduction to Physical Design Flow (Verilog coding, functional testing, adding physical constraints (timing, area, power, DFT, …), synthesis to cell library, timing analysis, placement and routing, clock synthesis, post-layout timing, I/O, Packaging and sign-off)	Tool Command Language (Tcl) and how to use it in Automating Digital Design Flow - 1
2	Logic Synthesis – 1 (design compilation strategies, library definitions, cell-based design, cell characterization, cell views, timing models, details of standard-cell libraries)	Tool Command Language (Tcl) and how to use it in Automating Digital Design Flow - 2
3	Logic Synthesis – 2 (Boolean minimization, Constraints definitions, technology mapping, synthesizable Verilog, timing optimization)	Synopsys flow overview, Synthesis 1 (Logic synthesis and standard cells)
4	Static Timing Analysis (Clocking circuits, timing constraints, path-based timing, block-based timing, slacks, yield, timing reports) + (Primetime SI) statistical timing analysis	Synthesis 2 (Design constraints, Optimization)
5	ASIC Physical Design – 1 (floor-planning, partitioning, hierarchical design, multiple-voltage domain, power planning)	STA -1 (STA VS simulation, Timing paths, required time, arrival time, slack, setup, hold)

6	ASIC Physical Design – 2 (placement: random, analytic, …)	STA -2 (Timing constraints, Timing reports) + CDC + Formal verification
7	Clock Tree Synthesis (clock distribution, clock generation, clock domain, implications of clocking)	ASIC 1 (data setup, Floorplanning)
8	Routing (goals, algorithms, constraints, global routing: definition, region assignment, pin assignment)	ASIC 2 (Power planning + placement)
9	I/O and Packaging (and introduction to 3D integration,UciE, …)	ASIC 3 (Placement, CTS)
10	Signoff and chip finishing (Parasitic Extraction, STA with SI, DRC/LVS, Post-layout Simulation, Power Analysis, DFT)	ASIC 4 (Grid Routing, Global Routing, Detailed Routing) + Signoff (STA)
11	Signal and Power Integrity;	